

Applicant: Yi-Bin Hsieh
Application No.: 10/810,016

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A duty cycle correction method for converting a pair of differential analog signals from an oscillator into an output pulse signal having the same frequency as that of each of said pair of differential analog signals and 50% duty cycle, said method comprising steps of:

processing said pair of differential analog signals into a first digital pulse signal and a second digital pulse signal, wherein said first digital pulse signal and said second digital pulse signal have a specified phase difference therebetween;

frequency-dividing said first digital pulse signal and said second digital pulse signal into a third digital pulse signal and a fourth digital pulse signal; and

generating said output pulse signal ~~according to~~ by performing an exclusive OR operation of said third and fourth digital pulse signals.

2. (Original) The duty cycle correction method according to claim 1 wherein said specified phase difference is 180 degrees.

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3. (Original) The duty cycle correction method according to claim 1 wherein said first digital pulse signal is frequency-divided by two to obtain said third digital pulse signal, and said second digital pulse signal is frequency-divided by two to obtain said fourth digital pulse signal.

4. (Cancelled)

5. (Currently Amended) A frequency synthesizing method, comprising steps of:

generating a pair of differential analog signals;

processing said pair of differential analog signals into a first digital pulse signal and a second digital pulse signal, wherein said first digital pulse signal and said second digital pulse signal have a specified phase difference therebetween;

frequency-dividing said first digital pulse signal and said second digital pulse signal into a third digital pulse signal and a fourth digital pulse signal ; and

generating an output pulse signal ~~according to~~ by performing an exclusive OR operation of said third and fourth digital pulse signals, wherein said output pulse signal having the same frequency as that of each of said pair of differential analog signals and 50% duty cycle.

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6. (Original) The frequency synthesizing method according to claim 5 wherein said differential analog signals have the same frequency and a phase difference of 180 degrees.

7. (Original) The frequency synthesizing method according to claim 5 wherein said first digital pulse signal is frequency-divided by two to obtain said third digital pulse signal, and said second digital pulse signal is frequency-divided by two to obtain said fourth digital pulse signal.

8. (Cancelled)

9. (New) A duty cycle correction method for converting a pair of differential analog signals from an oscillator into an output pulse signal, said method comprising steps of:

processing said pair of differential analog signals into a first digital pulse signal and a second digital pulse signal, wherein said first digital pulse signal and said second digital pulse signal have a specified phase difference therebetween, and the frequency of said first and second digital pulse signals is the same as that of said pair of differential analog signals;

frequency-dividing said first digital pulse signal and said second digital pulse

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signal into a third digital pulse signal and a fourth digital pulse signal, wherein the frequency of said third and fourth digital pulse signals is a fraction of that of said pair of differential analog signals; and

generating said output pulse signal having the same frequency as that of each of said pair of differential analog signals and 50% duty cycle according to said third and fourth digital pulse signals.

10. (New) The duty cycle correction method according to claim 9 wherein said differential analog signals have the same frequency and a phase difference of 180 degrees.

11. (New) The duty cycle correction method according to claim 9 wherein said first digital pulse signal is frequency-divided by two to obtain said third digital pulse signal, and said second digital pulse signal is frequency-divided by two to obtain said fourth digital pulse signal.

12. (New) The duty cycle correction method according to claim 9 comprising:
performing an exclusive OR operation of said third and fourth digital pulse signals for generating said output pulse signal.